Ultra Low Power Adiabatic Logic Using Diode Connected DC Biased PFAL Logic

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Abstract. *With the continuous scaling down of technology in the field of integrated circuit design, low power dissipation has become one of the primary focuses of the research. With the increasing demand for low power devices, adiabatic logic gates prove to be an effective solution. This paper briefs on different adiabatic logic families such as ECRL (Efficient Charge Recovery Logic), 2N-2N2P and PFAL (Positive Feedback Adiabatic Logic), and presents a new proposed circuit based on the PFAL logic circuit. The aim of this paper is to simulate various logic gates using PFAL logic circuits and with the proposed logic circuit, and hence to compare the effectiveness in terms of average power dissipation and delay at different frequencies. This paper further presents implementation of C17 and C432 benchmark circuits, using the proposed logic circuit and the conventional PFAL logic circuit to compare effectiveness of the proposed logic circuit in terms of average power dissipation at different frequencies. All simulations are carried out by using HSPICE Simulator at 65 nm technology at different frequency ranges. Finally, average power dissipation characteristics are plotted with the help of graphs, and comparisons are made between PFAL logic family and new proposed PFAL logic family.*

Keywords

Adiabatic logic, DCDB-PFAL, four phased power clock, low power, PFAL, power dissipation.

1. Introduction

The rapid advancement in semiconductor technology in electronic devices over the years has resulted in better performance and higher circuit densities. However, as the size is getting smaller and the integration density increases, the increasing power dissipation has become a primary concern for further development of VLSI circuit technology. The two main types of power dissipation in semiconductor devices are: static power and dynamic power dissipation. The dynamic power dissipation is due to the energy loss during the process of charging and discharging of output capacitance, during switching activities in transistor, while static power dissipation is caused by internal leakage in devices when the circuit is in off state [1].

Dynamic power dissipation has been the primary concern of circuit designers in early period. Various circuit technologies have been introduced for reducing dynamic power like sub-threshold logic [3], multi-threshold technology [4], and adiabatic logic circuit [2]. The adiabatic logic is a novel low power circuit technology which utilizes AC voltage supply as opposed to DC voltage supply so as to recycle the energy of circuits.

The term 'adiabatic' comes from 'thermodynamics' which is used to describe a process in which no energy exchanges with the environment, and hence no dissipation energy loss takes place. While in semiconductor devices, the charge transfer between different nodes is the process of energy exchange and different techniques can be used for minimizing this energy loss due to charge transfer. While fully adiabatic operation is the ideal condition of a circuit operation, in practical cases partial adiabatic operation of circuit is used because it gives considerable performance.

In conventional CMOS circuits the energy stored in load capacitors was dissipated to ground. While adiabatic logic, in contrast, offers a way to reuse this energy and thus prevents the wastage of this energy. By adding the ideas of both the conventional and the adiabatic logic circuits together, power dissipation can be reduced drastically.

Different circuits based on adiabatic logic have been proposed over the years [5], [6], [7] and [8]. To recycle the energy of circuit nodes, adiabatic logic based devices utilize AC power clock which has a four-phase operation. In these circuits the charge, rather flowing from the load capacitance to ground, it flows back to the trapezoidal or sinusoidal supply voltage and thus can be reused [9].

In this paper, power dissipation and delay is calculated for different logic gates using PFAL and with proposed PFAL logic, and results are compared graphically to see the effectiveness of the proposed logic circuit over the base PFAL adiabatic logic circuit. The rest of the paper is organized as follows: Section 2. overviews the conventional CMOS and adiabatic logic circuits. In Section 3. a proposed logic circuit is presented in brief and a 2:1 Multiplexer circuit is implemented using the proposed logic circuit. In Section 4. , simulation of circuits is done at different frequencies and results of power dissipation and propagation delay are compared and presented graphically. The paper ends with the conclusion given in Section 5.

2. Conventional CMOS and Adiabatic Logic

2.1. Conventional CMOS

In order to understand the conventional switching operation, a simple CMOS inverter is used. A pull-up and a pull-down MOS transistor, connected in series with a load capacitance C Fig. 1.

Power dissipation in CMOS transistors occurs mainly because of the device switching operations. At each charging and discharging operation, there is an inevitable energy loss of CV_{dd}^2 for static CMOS circuits. During charging operation, the energy dissipation through pull-up block from power supply is equal to CV_{dd}^2, of which half of the energy ($0.5\,CV_{dd}^2$) is stored in load capacitor. The other half is dissipated through the resistive path, and lost as heat to the environment. Now during the operation of discharging, the residual energy stored in the load capacitor ($0.5\,CV_{dd}^2$) will be released to the ground through pull-down network [11]. And therefore, no energy recovery is possible in the conventional CMOS circuits.

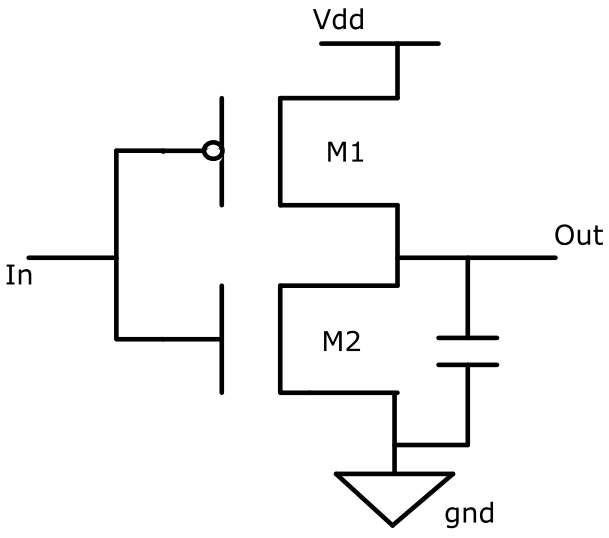

Fig. 1: Conventional CMOS inverter.

2.2. Adiabatic Logic

The use of AC power clock as opposed to DC supply makes the adiabatic circuits capable of recovering the stored energy of node capacitors back to the power source, and hence avoids the dynamic power loss almost completely, theoretically. The use of adiabatic logic principle in designing low power circuits is continuously growing and is proving to be a better selection in comparison to other conventional circuits. The adiabatic operation usually consists of four phases, with a phase difference of one quarter of a period. The four phases of operation respectively are Wait, Evaluate, Hold and Recovery Fig. 2. In the WAIT phase the power clock stays at low (zero) value, which maintains the outputs at low value, and the evaluation logic generates pre-evaluated results. Now, since the power clock is at low level, the pre-evaluated inputs will not affect the state of the gate. In the EVALUATE phase, the power supply ramps up from zero to V_{dd} gradually, and the outputs will be evaluated as per the result of pre-evaluation logic. In the HOLD phase, power clock stays high, providing the constant input signal for the next stage in pipelining of adiabatic circuits, and keep the outputs valid for the entire phase. Meanwhile inputs ramp down to low value. In the RECOVERY phase of operation, the power supply ramps down to zero and the energy of the circuit nodes is recovered back to the power source instead of being dissipated as heat [6].

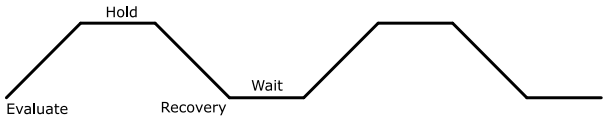

Fig. 2: Four hased trapezoidal power clock.

2.3. Efficient Charge Recovery Logic (ECRL)

Efficient Charge Recovery Logic (ECRL) [5], as shown in Fig. 3, uses two PMOS transistors in cross-coupled

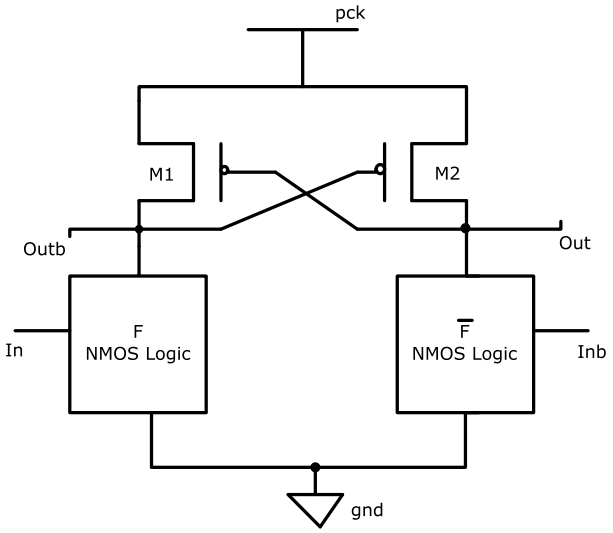

Fig. 3: Efficient charge recovery logic (ECRL).

fashion, and two NMOS transistors in the N-functional blocks of ECRL logic block. In order to recover the supplied energy which can be reused, ECRL gates use AC power clock (pck). Let us assume, input '**In**' is at high level and '**Inb**' is at low level. At the beginning of a cycle, when power clock 'pck' rises from zero to V_{dd}, '**Out**' remains at low level because the high input '**In**' turns the F NMOS logic high. Output '**Outb**' follows the power clock 'pck' through M1. Now when 'pck' reaches to V_{dd}, the outputs hold valid logic values. During the hold phase these output values are maintained and can be used as inputs for evaluation of the next stage. In the next phase of recovery, the power clock falls down to zero level and the energy from the output node can be returned to the 'pck' so as to recover the delivered charge [13]. The major disadvantage of this circuit is the existence of coupling effects, since the two outputs are driven by the PMOS latch, and so the two complementary outputs may interfere with each other.

2.4. 2N-2N2P Logic

2N-2N2P Logic family is a variation of ECRL Logic family with two new cross coupled NMOS transistors added parallel to the 2 existing NMOS transistors. The generalized 2N-2N2P circuit diagram is shown in Fig. 4. And as the operation is concerned, it is identical to that of ECRL family. This new family is derived in order to reduce the coupling effects in the circuit. Also, the two new NMOS transistors have the advantage of eliminating the floating nodes for large part of the recovery phase. However, the added transistors prevent the circuits form achieving significant power reduction as compared to the ECRL logic circuits [10].

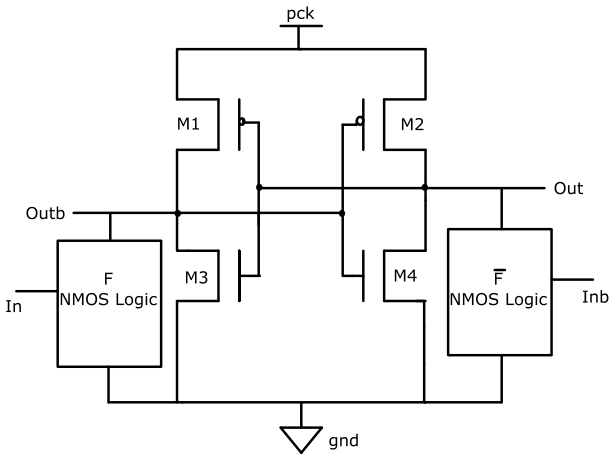

Fig. 4: 2N-2N2P basic logic circuit.

2.5. Positive Feedback Adiabatic Logic (PFAL)

The Positive Feedback Adiabatic Logic (PFAL) achieves the lowest power consumption as opposed to other similar adiabatic logic families. The generalized PFAL circuit diagram is shown in Fig. 5. The latch is made similar to the 2N-2N2P logic circuit with two PMOS transistors and two NMOS transistors. The functional blocks of NMOS logic are connected in parallel with the PMOS transistors of the latch and form the transmission gates. The fact that the functional blocks are in parallel with the PMOS transistors, the equivalent resistance is smaller during the charging of capacitance [13].

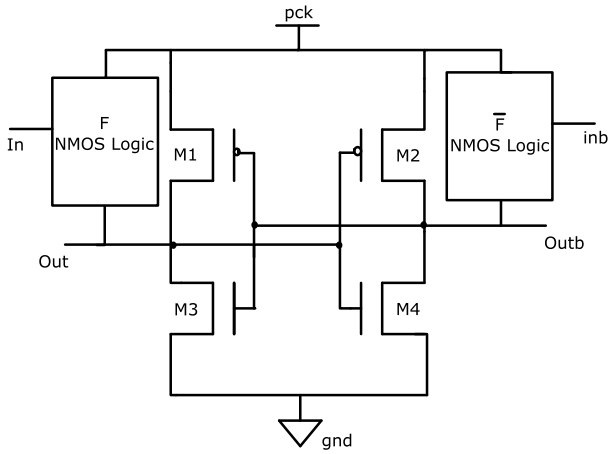

Fig. 5: PFAL basic logic circuit.

3. Proposed Circuit

The generalized circuit diagram for the proposed logic is shown in Fig. 6. The circuit is similar to PFAL logic circuit with the latch comprising of two PMOS

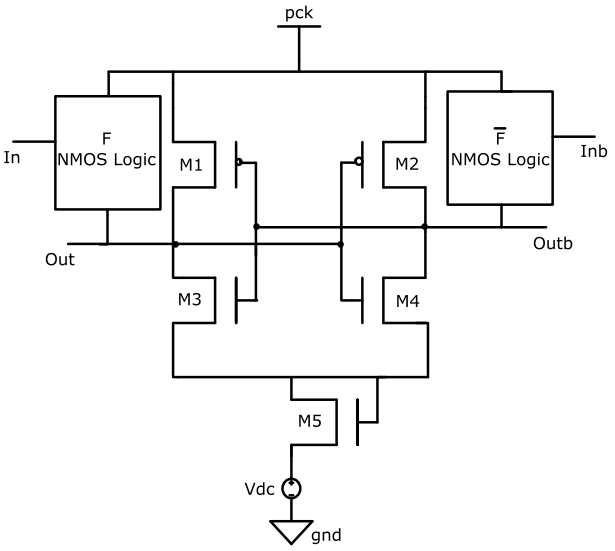

Fig. 6: DCDB-PFAL basic circuit.

transistors and two NMOS transistors. The functional blocks of NMOS logic are connected in parallel with the PMOS transistors of the latch forming the transmission gates similar to PFAL logic. The difference lies in the pull-down block with an NMOS diode and a DC voltage source connected between the pull-down NMOS transistors and the ground. The idea behind the use of a diode at the bottom of NMOS tree is that it will help in controlling the discharging path by decreasing the rate of discharge of internal nodes of the logic circuit. And to further incorporate the advantage of level shifting technique, a positive DC voltage source is connected between the diode and the ground. The level shifting technique reduces the gate to source voltage at the output transistors and reduce gate current and leakage current. This DC voltage source is varied in the range of 0.1 V to 0.3 V and simulations are done.

The effect of connecting an active load and a DC voltage source needs to be understood in order to analyze the proposed logic effectively. As we know from the basic concept of MOSFET that in an NMOS transistor with its drain terminal shorted to gate terminal, it will always be working in the saturation region.

As, $V_{ds} = V_{gs}$. Therefore, $V_{DS} > V_{GS} - V_T$ always and thus it is in saturation region. That is the NMOS diode is always on for all $V_{GS} \geqq V_T$ values. And the current IDS will be given by:

$$I_{DS} = K(V_{GS} - V_T)^2 = K(V_{DS} - V_T)^2. \quad (1)$$

From the equation it can be seen that IDS is now dependent on VDS squarely. In our proposed DCDB-PFAL logic, the source terminal of the NMOS diode is connected to a positive DC voltage source of value V_{dc} which is then connected through ground terminal. Thus we see that the source voltage $V_S = V_{dc}$. And so, $V_{DS} = V_D - V_{dc}$. Therefore, Eq. (1) will now become:

$$I_{DS} = K(V_{DS} - V_T)^2 = K((V_D - V_{dc}) - V_T)^2. \quad (2)$$

From Eq. (2) it can be seen that, as we apply a positive voltage at DC source, V_{DS} will start reducing. As a result, $V_{DS} - V_T$ will reduce and thus I_{DS} will start reducing. Therefore, we can see that with the use of an NMOS diode and with increasing the DC voltage both the voltage difference and the current start reducing. And thus a further reduction in power dissipation is achieved with the new proposed DCDB-PFAL technology of adiabatic logic family. The circuit attains low-power operation because a low DC Source is connected to the circuit in series. Thus the proposed logic family reduces the gate to source voltage at the output transistors and thus reducing the gate and leakage current and providing further lower power dissipation as compared to conventional PFAL logic circuit. A 2:1 MUX has been implemented using conventional PFAL and proposed DCDB-PFAL logic. Circuit diagrams for both of them are shown in Fig. 7 and Fig. 8 respectively.

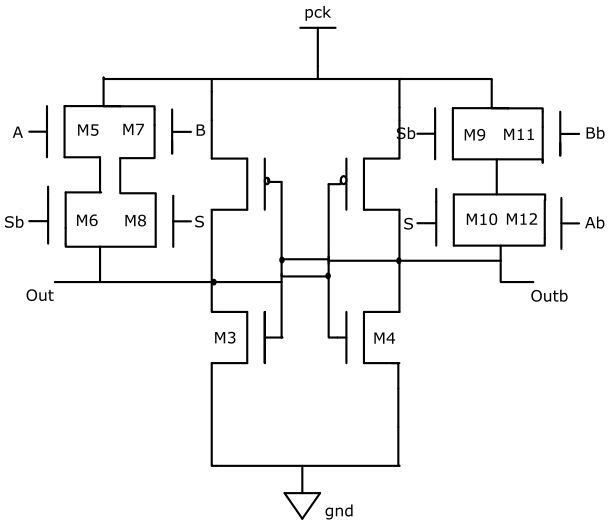

Fig. 7: 2:1 MUX using conventional PFAL.

In Fig. 9 and Fig. 10 we have shown the waveforms for implemented combinational circuits using conventional PFAL logic and by using proposed logic family, respectively at 100 MHz frequency. The graph shows the waveform for power clock used, inputs A and B, select line S and the output waveform. The effect of using a dc source can be seen from the output waveform of Fig. 10, where the output voltage is not zero but it is level shifted by the value of the V_{dc} which is varied in between 0.1 V to 0.3 V.

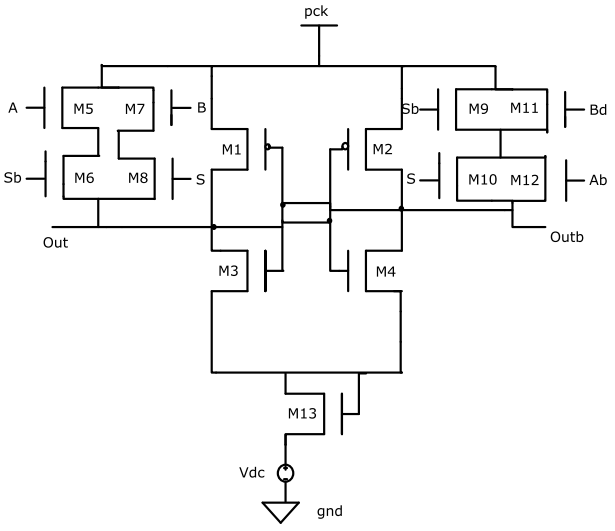

Fig. 8: 2:1 MUX using proposed DCDB-PFAL.

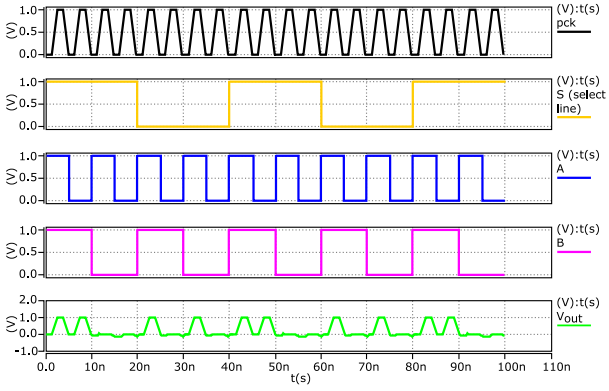

Fig. 9: Input/Output waveforms for PFAL 2:1 MUX at 100 MHz.

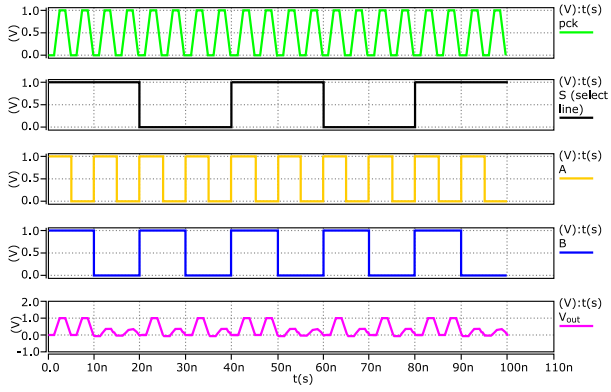

Fig. 10: Input/Output waveforms for DCDB-PFAL 2:1 MUX at 100 MHz.

4. Simulation and Result

In order to see the effectiveness of the proposed DCDB-PFAL logic circuits over conventional PFAL logic family, different logic gates have been implemented, first using conventional PFAL logic family and then by using proposed DCDB-PFAL logic as discussed in this paper. Finally, a 2:1 Multiplexer circuit is implemented and average power and delay calculations are made at different frequencies and different DC voltages for the voltage source.

Tab. 1: Design parameters.

TYPE	PFAL	Proposed DCDB -PFAL
PMOS (width)	260 nm	260 nm
NMOS (width)	130 nm	130 nm
DC values (Vdc) for proposed logic	––	0.1 V to 0.3 V
Power clock (pck)	1 V Trapezoidal Power Clock	
Frequency	100 MHz, 500 MHz, 1 GHz	

All the logic circuits are simulated using HSPICE Simulator at 65 nm technology. Table 1 lists the design parameters utilized in the simulation of circuits, and Tab. 2, Tab. 3, Tab. 4, Tab. 5 and Tab. 6 show the results of power dissipation, delay and power delay product (PDP) for different logic circuits. Finally, the graphs have been plotted, showing the comparison of average power dissipation for the PFAL and DCDB-PFAL circuit. We have shown the waveforms of simulation of 2:1 MUX using PFAL and DCDB-PFAL logic families. Further, Fig. 11, Fig. 12, Fig. 13 show an average power comparison for 2:1 MUX circuit using proposed circuit over PFAL, while Fig. 14, Fig. 15, Fig. 16 show a comparison of lowest power dissipation achieved using proposed DCDB-PFAL circuits over conventional PFAL circuits.

It can be seen from the readings of different tables and different graphs plotted for different logic circuits at different frequencies that with the dc voltage varying between 0.1 V to 0.3 V, power first decreases up till around 0.25 V and then increases gradually. And the proposed circuit performs better in comparison to the conventional adiabatic families up to a voltage range of 0.3 V Vdc. The DCDB-PFAL INVERTER consumes 48% less power as compared to PFAL INVERTER. The

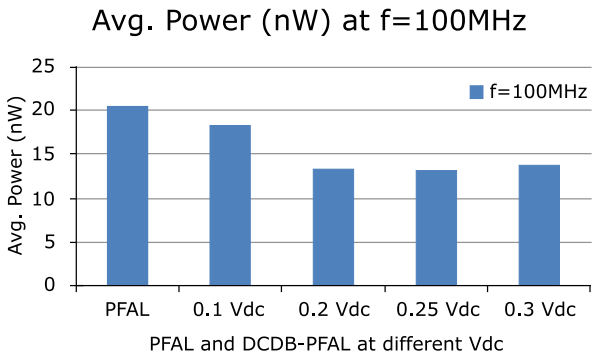

Fig. 11: Average power comparison of conventional PFAL vs. proposed DCDB-PFAL 2:1 MUX at 100 MHz.

Tab. 2: Performance comparison of PFAL and proposed DCDB-PFAL INVERTER circuit.

Frequency (MHz)	Parameters	PFAL Inverter	DCDB-PFAL Inverter at different Vdc			
			0.1V	0.2V	0.25V	0.3V
100	Avg. Power (nW)	11.93	11.04	6.754	6.093	6.469
	Delay (ns)	1.249	1.251	1.25	1.25	1.249
	PDP (fWs)	0.019	0.018	0.008	0.007	0.008
500	Avg. Power (nW)	126.7	105.5	96.94	95.61	98.37
	Delay (ns)	0.25	0.25	0.25	0.25	0.249
	PDP (fWs)	0.031	0.026	0.024	0.023	0.024
1000	Avg. Power (nW)	422.3	368.8	353.5	353.5	354.3
	Delay (ns)	0.12	0.12	0.118	0.119	0.119
	PDP (fWs)	0.05	0.044	0.041	0.042	0.042

Tab. 3: Performance comparison of PFAL and proposed DCDB - PFAL AND/NAND circuit.

Frequency (MHz)	Parameters	PFAL AND/ NAND	DCDB-PFAL AND/NAND at different Vdc			
			0.1V	0.2V	0.25V	0.3V
100	Avg. Power (nW)	13.77	13.01	8.223	7.817	8.515
	Delay (ns)	1.245	1.247	1.246	1.246	1.244
	PDP (fWs)	0.017	0.016	0.01	0.009	0.01
500	Avg. Power (nW)	126.6	117.2	107.4	106	111.4
	Delay (ns)	0.245	0.245	0.245	0.244	0.244
	PDP (fWs)	0.031	0.028	0.026	0.025	0.027
1000	Avg. Power (nW)	418.4	391.6	380.3	382.3	388.2
	Delay (ns)	0.12	0.124	0.124	0.124	0.125
	PDP (fWs)	0.05	0.048	0.047	0.047	0.048

Tab. 4: Performance comparison of PFAL and proposed DCDB - PFAL OR/NOR circuit.

Frequency (MHz)	Parameters	PFAL OR/ NOR	DCDB-PFAL OR/NOR at different Vdc			
			0.1V	0.2V	0.25V	0.3V
100	Avg. Power (nW)	13.51	12.68	8.441	8.191	9.028
	Delay (ns)	1.245	1.218	1.245	1.201	1.201
	PDP (fWs)	0.016	0.015	0.01	0.009	0.011
500	Avg. Power (nW)	125.5	114.3	112.8	111.9	116.1
	Delay (ns)	0.246	0.236	0.236	0.238	0.237
	PDP (fWs)	0.031	0.027	0.026	0.026	0.027
1000	Avg. Power (nW)	438.7	409.4	412.4	414.3	418.6
	Delay (ns)	0.121	0.119	0.116	0.118	0.119
	PDP (fWs)	0.053	0.049	0.048	0.049	0.049

Tab. 5: Performance comparison of PFAL and proposed DCDB- PFAL XOR/XNOR circuit.

Frequency (MHz)	Parameters	PFAL XOR/ XNOR	DCDB-PFAL XOR/XNOR at different Vdc			
			0.1V	0.2V	0.25V	0.3V
100	Avg. Power (nW)	26.32	24.83	18.82	18.51	19.15
	Delay (ns)	1.246	1.246	1.245	1.243	1.244
	PDP (fWs)	0.032	0.031	0.023	0.023	0.023
500	Avg. Power (nW)	228.1	209.1	204.1	201.2	206.7
	Delay (ns)	0.246	0.244	0.244	0.244	0.244
	PDP (fWs)	0.056	0.051	0.049	0.049	0.051
1000	Avg. Power (nW)	732.2	675.1	670.1	673.3	679.2
	Delay (ns)	0.121	0.123	0.124	0.123	0.123
	PDP (fWs)	0.089	0.083	0.083	0.083	0.083

Tab. 6: Comparison of PFAL and proposed DCDB-PFAL 2:1 MUX circuit.

Frequency (MHz)	Parameters	PFAL 2:1 MUX	DCDB-PFAL 2:1 MUX at different Vdc			
			0.1V	0.2V	0.25V	0.3V
100	Avg. Power (nW)	20.586	18.45	13.42	13.3	13.77
	Delay (ns)	1.2556	1.25	1.228	1.231	1.233
	PDP (fWs)	0.0258	0.023	0.016	0.016	0.017
500	Avg. Power (nW)	183.76	181.1	176.2	174.5	176.6
	Delay (ns)	0.2549	0.254	0.255	0.255	0.254
	PDP (fWs)	0.0468	0.046	0.045	0.044	0.045
1000	Avg. Power (nW)	659.9	602.6	600.2	601.5	606.5
	Delay (ns)	0.1313	0.123	0.123	0.123	0.123
	PDP (fWs)	0.0866	0.074	0.074	0.074	0.074

proposed NAND gate consumes 43.24 % less power as compared to PFAL NAND gate. Proposed NOR gate consumes 39 % less power as compared to PFAL NOR gate. XOR gate consumes 29 % less power as compared to PFAL XOR gate. And proposed 2:1 MUX consumes 35 % less power as compared to PFAL logic. Also by observing the readings from different tables, it is observed that for a particular logic circuit, delay remains nearly constant at a particular frequency as dc voltage is varied from 0.1 V to 0.3 V. That is, the proposed DCDB-PFAL logic family provides much lower power dissipation without affecting the speed of operation of the logic circuit as compared to that of conventional PFAL adiabatic logic family.

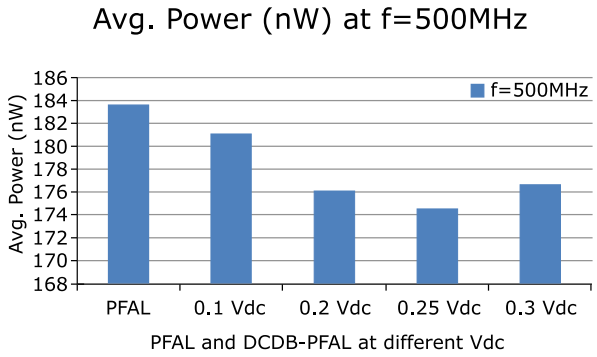

Fig. 12: Average power comparison of conventional PFAL vs. proposed DCDB-PFAL 2:1 MUX at 500 MHz.

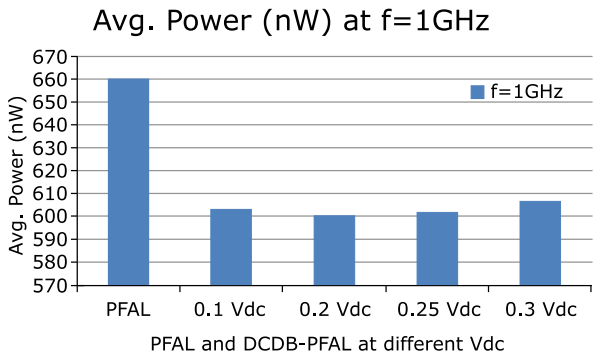

Fig. 13: Average power comparison of conventional PFAL vs. proposed DCDB-PFAL 2:1 MUX at 1 GHz.

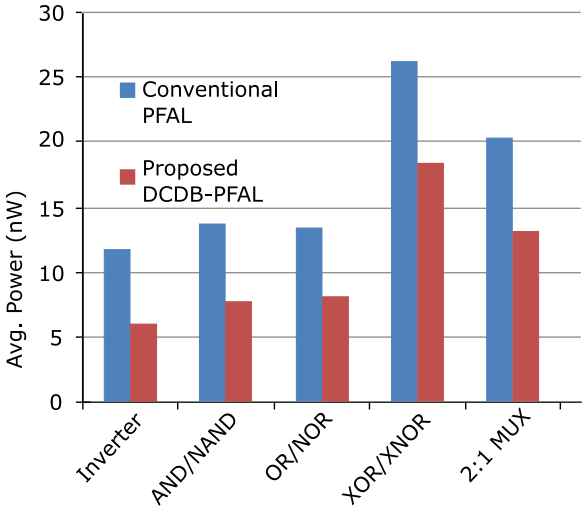

Fig. 14: Graph showing lowest power achieved for different logic gates using proposed DCDB-PFAL over conventional PFAL at 100 MHz.

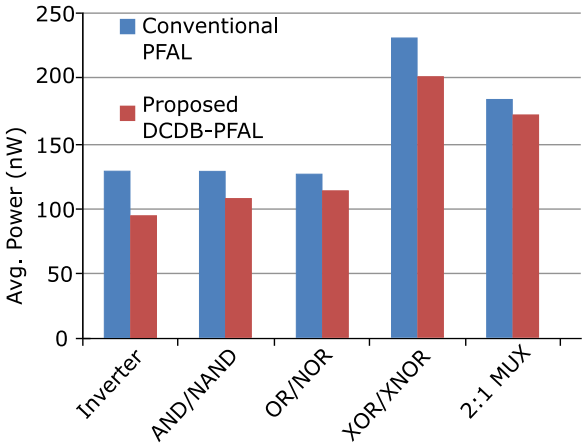

Fig. 15: Graph showing lowest power achieved for different logic gates using proposed DCDB-PFAL over conventional PFAL at 500 MHz.

Tab. 7: Performance comparison of PFAL and proposed DCDB - PFAL AND/NAND circuit.

Frequency (MHz)	Parameters	# Gates	PFAL AND/ NAND	Average Power (μW) DCDB-PFAL AND/NAND at different Vdc			
				0.1V	0.2V	0.25V	0.3V
100	C17	6	23.46	22.86	16.43	15.76	16.89
500			136.2	124.7	109.4	107.1	111.6
1000			463.4	418.2	409.8	408	409.4
100	C432	261	1267	1092	981	977	995
500			2623	2527	2236	2225	2274
1000			4456	4209	4117	4063	4179

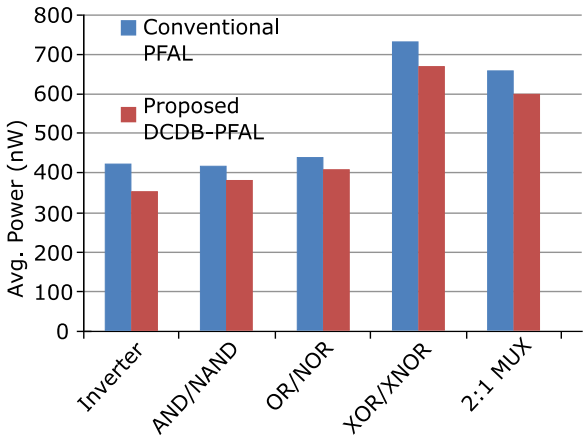

Fig. 16: Graph showing lowest power achieved for different logic gates using proposed DCDB-PFAL over conventional PFAL at 1 GHz.

For proper validation and verification of the results we have tested our existing and proposed work on bechmark circuits C17 and C432 as shown in Fig. 17 The results for average power dissipation of the benchmark circuits are shown in Tab. 7. C17 benchmark circuit provides a percentage improvement of 32 % in power dissipation for DCDB-PFAL logic over PFAL logic based circuit. While for the C432 benchmark circuit a power reduction of 22 % is achieved for the DCDB-PFAL logic circuit over the conventional PFAL based benchmark circuit.

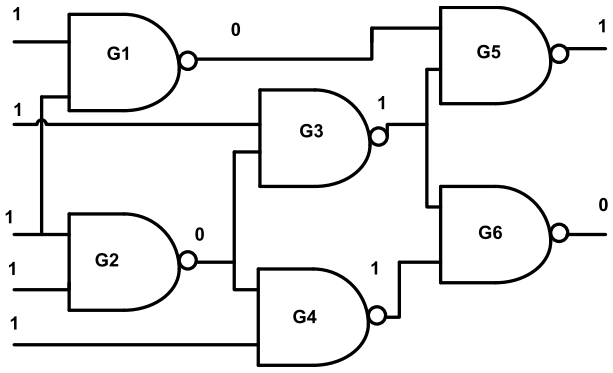

Fig. 17: C17 benchmark circuit using NAND gates.

5. Conclusion

This paper reviews the basic adiabatic logic circuits. Different logic gates have been implemented using the proposed DCDB-PFAL logic and conventional PFAL logic at different frequencies and for different values of dc voltages for the new logic circuit. Besides, a combinational circuit 2:1 MUX has also been implemented for the proposed and the conventional logic. Finally, we have further implemented benchmark circuits C17 and C432 for further validation of the proposed DCDB-PFAL logic family. The results show much enhanced performance of the proposed circuit over conventional PFAL logic and it offers significant power reduction over the PFAL. DCDB-PFAL based C17 benchmark circuit provides 32 % lower power dissipation while DCDB-PFAL based C432 benchmark circuit provides 22 % lower power dissipation as compared to the conventional PFAL based benchmarks circuits respectively. It can be seen from the tables and different graphs plotted, that as the dc voltage is varied between 0.1 V to 0.3 V, power first decreases up till around 0.25 V and then increases gradually. The proposed DCDB-PFAL logic can be used in devices which need to work on ultra-low power such as pacemaker, hearing machine and other medical purpose devices. As the quest for ultra-low power circuit designs keep on increasing, these improved circuit technologies would prove to be very useful in serving the need.

References

[1] KEOTE, M. L. and P. T. KARULE. Design and Implementation of Energy Efficient Adiabatic ECRL and Basic Gates. In: *International Conference on Soft Computing Techniques and Implementations (ICSCTI)*. Faridabad: IEEE, 2015, pp. 87–91. ISBN 978-1-4673-6792-9. DOI: 10.1109/ICSCTI.2015.7489543.

[2] DENKER, J. S. A review of adiabatic computing. In: *IEEE Symposium on Low Power Electronics*. San Diego: IEEE, 1994, pp. 94–97. ISBN 0-7803-1953-2. DOI: 10.1109/LPE.1994.573218.

[3] CALHOUN, B. H., S. KHANNA and R. MANN. Sub-threshold circuit design with shrinking CMOS devices. In: *IEEE International Symposium on Circuits and Systems*. Taipei: IEEE, 2009, pp. 2541–2544. ISBN 978-1-4244-3827-3. DOI: 10.1109/ISCAS.2009.5118319.

[4] HEMANTHA, S., A. DHAWAN and K. HARANATH. Multi-threshold CMOS design for low power digital circuits. In: *IEEE Region 10 Conference TENCON*. Hyderabad: IEEE, 2008, pp. 1–5. ISBN 978-1-4244-2408-5. DOI: 10.1109/TENCON.2008.4766689.

[5] MOON, Y. and D. K. JEONG. Efficient charge recovery logic. In: *Symposium on VLSI Circuits, Digest of Technical Papers*. Kyoto: IEEE, 1995, pp. 129–130. ISBN 0-7800-2599-0. DOI: 10.1109/VLSIC.1995.520719.

[6] KRAMER, A., J. S. DENKER, B. FLOWER and J. MORONEY. 2nd order adiabatic computing with 2N-2N and 2N-2N2P logic circuits. In: *Proceedings of the International Symposium on Low Power Design*. Dana Point: ACM, 1995, pp. 191–196. ISBN 0-89791-744-8. DOI: 10.1145/224081.224115.

[7] VETULI, A., S. D. PASCOLI and L. M. REYNERI. Positive feedback in adiabatic logic. *Electronic Letters*. 1996, vol. 32, iss. 20, pp. 1867–1869. ISSN 0013-5194. DOI: 10.1049/el:19961272.

[8] BLOTTI, A., S. D. PASCOLI and R. SALETTI. Simple model for positive feedback adiabatic logic power consumption estimation. *Electronic Letters*. 2000, vol. 36, iss. 2, pp. 116–118. ISSN 0013-5194. DOI: 10.1049/el:20000183.

[9] YIBIN, Y. and R. KAUSHIK. Ultra Low Energy Computing using Adiabatic Switching Principle. *Purdue e-Pubs* [online]. 1995. Available at: `http://docs.lib.purdue.edu/ecetr/114`

[10] CHAUDHURI, A., M. SAHA, M. BHOWMIK, S. N. PRADHAN and S. DAS. Implementation of Circuit in Different Adiabatic Logic. In: *International Conference on Electronics and Communication System*. Coimbatore: IEEE, 2015, pp. 353–359. ISBN 978-1-4799-7225-8. DOI: 10.1109/ECS.2015.7124923.

[11] LIAO, N., X. CUI, K. LIAO, K. MA, D. WU, W. WEI, R. LI and D. YU. Low power adiabatic logic based on FinFETs. *Science China Information Sciences*. 2014, vol. 57, iss. 2, pp. 1–13. ISSN 1869-1919. DOI: 10.1007/s11432-013-4902-x.

[12] KUSHAWAHA, S. P. S. and T. N. SASAMAL. Modified Positive Feedback Adiabatic Logic for Ultra Low Power VLSI. In: *International Conference on Computer, Communication and Control*. Indore: IEEE, 2015, pp. 1–5. ISBN 978-1-4799-8164-9. DOI: 10.1109/IC4.2015.7375579.

[13] SHINGHAL, D., A. SAXENA and A. NOOR. Adiabatic Logic Circuits: A retrospective. *MIT International Journal of Electronics and Communication Engineering*. 2013, vol. 3, iss. 2, pp. 108–114. ISSN 2230-7672.

[14] SINGH, R., A. SHARMA and R. SINGH. Power Efficient Design of Multiplexer based Compressor using Adiabatic Logic. *International Journal of Computer Applications*. 2013, vol. 81, iss. 10, pp. 45–50. ISSN 0975-8887. DOI: 10.5120/14052-2217.

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